Matrix Series

MIL-DTL-38999 Optical Transceiver, GbE, FC, ARINC 818 or sFPDP Applications, Multimode, 850nM

8xTX & 8xRX or 16TX or 16RX, Flange Mount

8xTX & 8xRX or 16TX or 16RX lines operating from 0.125 to 5.0Gbps

FEATURES

- Suitable for GbE, Fibre Channel, ARINC 818 and sFPDP applications at up to 5.0Gbps
- Optical fiber link distances up to 550 Meters (50/125µ 2000MHz*Km MMF)
- Maximum optical channel bit error rate less than $1x10^{-12}$
- Operating temperature range from -40°C to +85°C
- Shock, vibration and immersion resistant per MIL-STD-810 and Mil-Std-1344
- Aluminum alloy D8999 housings are strong, durable, corrosion resistant and light weight
- M29504 compliant optical fiber connector interface

APPLICATIONS

Matrix series bulkhead mounted optical transceivers enable extremely high speed network communications over long distances in harsh environments.

- Gigabit Ethernet switches and peripherals
- Fibre Channel switches and peripherals
- Video displays and display drivers
- High speed sensor data links

The MIL-DTL-38999, Series III shell provides a sealed optical interface that is water-tight to Mil-Std-810 / IP67 / NEMA-4x when mated.

The multimode optical fiber interface supports applications where copper cable link distance, bandwidth, weight or bulk make the use of twisted pair, twinax or quadrax copper conductors unacceptable.

DESCRIPTION

Matrix series octal port (16xfiber) optoelectronic transceivers consist of up to 8 total optical transmitter and receiver functions (or 16 transmitter or 16 receive) integrated into a bulkhead mounted MIL-DTL-38999, Series III receptacle connector. The optical transmitters are 850nm VCSEL lasers. The transmitter input lines are driven with differential CML signals applied to the transmitter (TX+ and TX-) lines. Dual loop, temperature compensated, VCSEL drivers convert the transmitter input signals to suitable VCSEL bias and modulation currents.

The optical receivers consist of PIN and preamplifier assemblies and limiting post-amplifiers. Outputs from the receivers consist of differential CML data signals on the receiver (RX+ and RX-) lines and single ended CMOS indicator functions on the Loss of Signal (LOS) lines. The receiver data lines are squelched upon LOS assertion, preventing errant data generation when an invalid incoming optical signal is presented to the transceiver.

The electrical interface to the Matrix series optical fiber transceivers is a controlled impedance connector enabling interface to a ribbon coax or twinax cable or flexible printed circuit assembly.

Matrix series octal port optical fiber transceivers are vibration isolated, environmentally hardened components designed for use in harsh environment applications.

- Panel mounted D38999 interface sealed against liquid and solid contaminants
- Shock and vibration resistant

ORDERING INFORMATION

Application	Part Number
8xTX & 8xRX - 5.0Gbps	T38F-PS1K-Hx

See Appendix A2 for other part number options

MOOG

ABSOLUTE MAXIMUM RATINGS

Absolute maximum limits mean that no catastrophic damage will occur if the product is subjected to these ratings for short periods, provided each limiting parameter is in isolation and all other parameters have values within the performance specification. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time.

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Storage Temperature	T_S	-55		+100	°C
Supply Voltage	V_{CC}	-0.3		+3.8	V
TX_DIS Input Voltage	V_I	-0.5		V_{CC} + 0.5	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating Temperature	T_A	-40		+85	°C
Supply Voltage	V_{CC}	+3.135		+3.465	V
TX Common Mode Voltage	V_{CM}		2.0		V
TX Differential Input Voltage (p-p)	V_D	0.25		2.2	V
Power Supply Noise (p-p)	N_P			200	mV

SPECIFICATIONS COMPLIANCE

Requirement	Feature	Condition	Notes
MIL-STD-883	ESD	Class II	2200V
MIL-STD-810	Vibration	$3.8g^2/Hz$	43G rms
MIL-STD-810	Shock	40.0g	6-9mS
MIL-STD-810	Immersion	1.0 meter	2 .0Hours
MIL-STD-1344	Flame Resistance	Method 1012	30 Seconds
MIL-STD-1344	Damp Heat	10 Cycles	24 Hours
MIL-STD-38999	Mating Durability	500 Cycles	<0.5dB Change
FDA / CDRH / IEC-825-1	Eye Safety	Class 1	No Safety Interlocks Required

MATERIALS

Item	Detail	Notes
Housing & Shell	Aluminum Alloy	
Housing & Shell Plating	Electroless Nickel or OD-CD	
Insert	Thermoplastic	
Interfacial Seal	Elastomer	
Optical Ferrules	Ceramic	
Printed Circuits	Polyimide / FR-4	

OPTICAL TRANSMITTERS T_A = Operating Temperature Range, V_{CC} = 3.135V to 3.465V

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Optical Output Power (BER<10^{-12}, PRBS= 2^7-1)	P_o	-6.5		-1.0	dBm
Optical Output Wavelength	λ_{OUT}	830	850	860	nM
Spectral Width	$\Delta\lambda_{RMS}$			0.85	nM
Extinction Ratio	ER	3.0	5.5		dB

OPTICAL RECEIVERS T_A = Operating Temperature Range, V_{CC} = 3.135V to 3.465V

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Optical Sensitivity (BER<10^{-12}, ER=5.0dB) 125Mbps to 5.0Gbps	P_I	-14.0		0.0	dBm
Optical Wavelength	λ_{IN}	830		860	nM

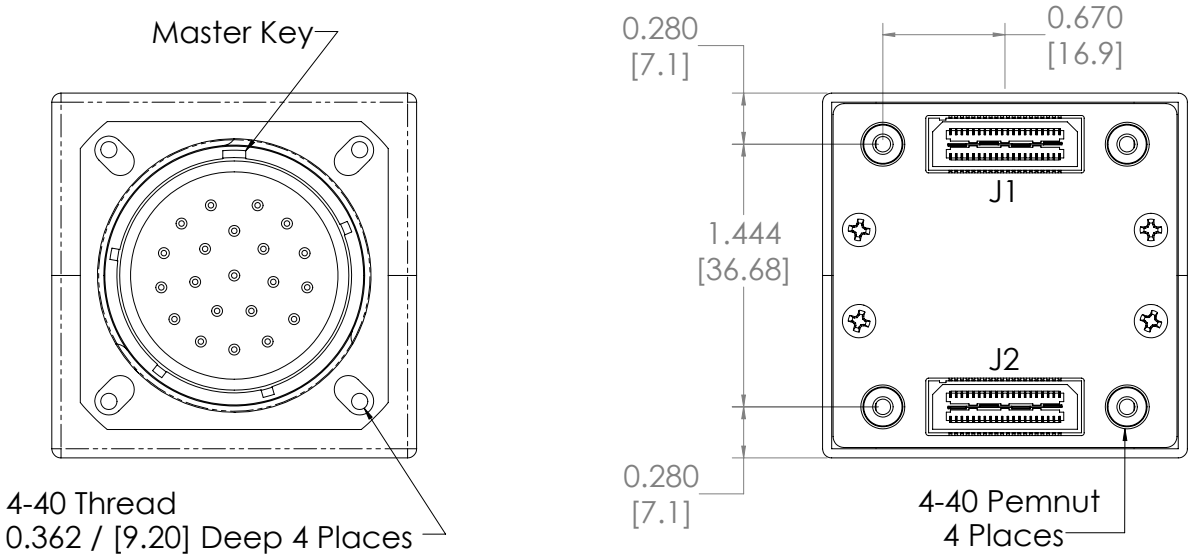
POWER SUPPLY CURRENT T_A = Operating Temperature Range, V_{CC} = 3.135V to 3.465V

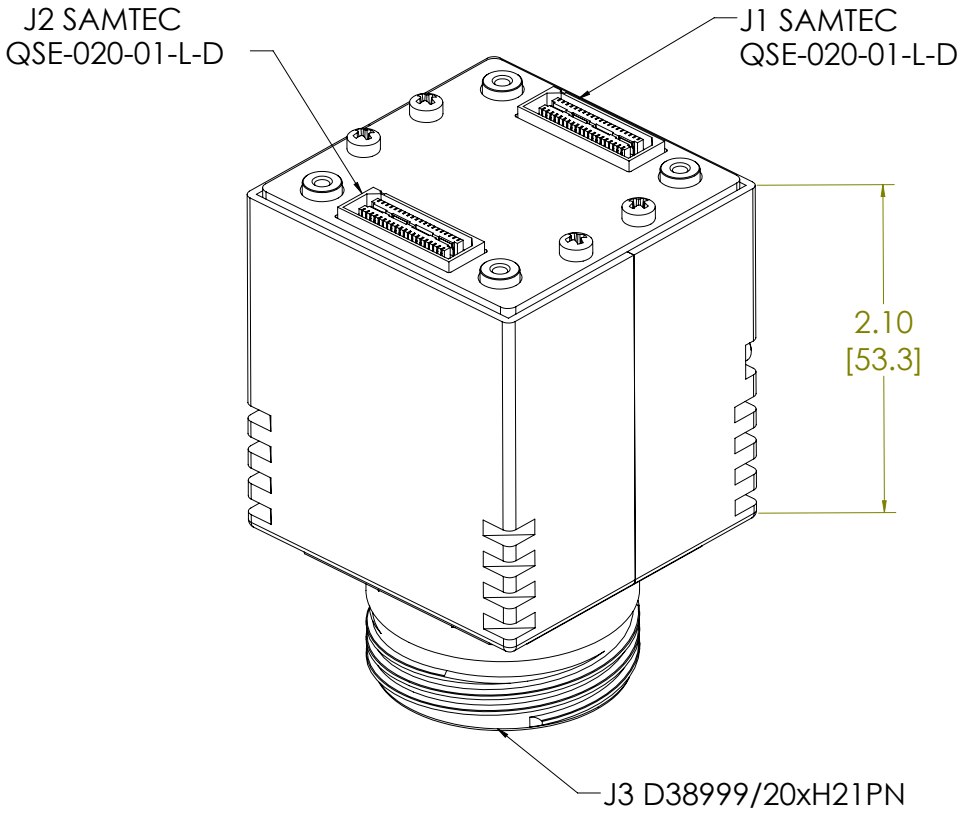
Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Current per each element	I_{CCT}		90	100	mA

Matrix Series MIL-DTL-38999 Optical Transceiver,
Gigabit Ethernet, Fibre Channel, ARINC 818 Applications, Multimode, 850nM

OUTLINE DRAWING

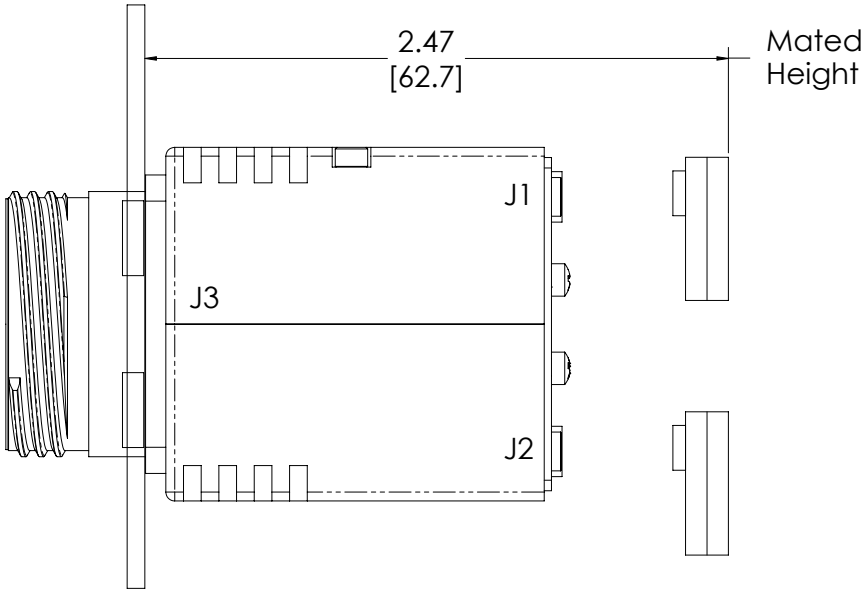
Dimensions are shown as: inches (mm)

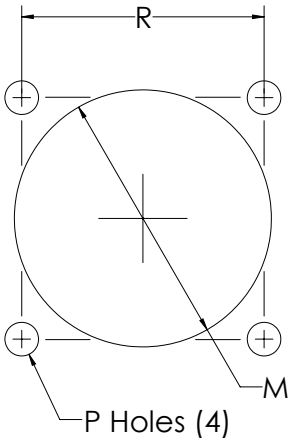




PANEL MOUNTING REQUIREMENTS

Dimensions are shown as: inches (mm)



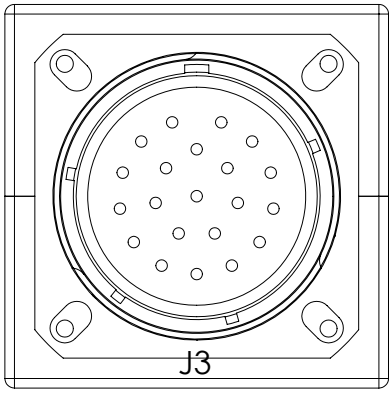


Panel Cutout Dimensions
Rear Panel Mounting Only

Shell Size Code	Shell Size	M Min	P Holes	R Bsc
H	23	1.547 (39.29)	0.159 (4.0) 0.149 (3.8)	1.375 (34.9)

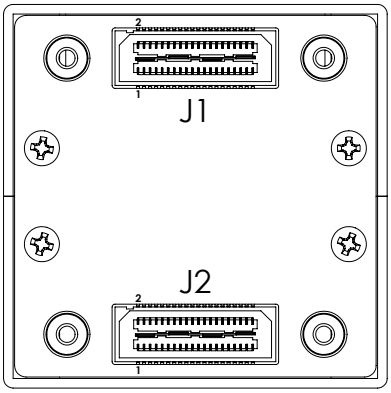
OPTICAL TRANSCEIVER INSERT ARRANGEMENT

TOP
Optical Interface



Front face of the optical transceiver insert shown, fiber optic cable plug opposite - see Appendix A1 for details

TOP
Electrical Interface



Back face of the optical transceiver shown - see Electrical Pin Assignment pages for details

OPTICAL TRANSCEIVER PORT ASSIGNMENTS

Electrical Connector J1 / J2	J3 Optical Pin Assignment
J1	B
	A
	N
	M
	C
	R
	W
	L
J2	D
	S
	V
	K
	E
	F
	H
	J

Matrix Series MIL-DTL-38999 Optical Transceiver,
Gigabit Ethernet, Fibre Channel, ARINC 818 Applications, Multimode, 850nM

J1 ELECTRICAL PIN ASSIGNMENTS - 8TX + 8RX pattern indicated

*J1 Pin #	Symbol	I/O	J3 Pin #	Description	Logic Family
1	V_{CC}	I	All	3.3VDC	N/A
2	TX_Dis	I	B	Transmitter Disable	LVTTL
3	V_{CC}	I	All	3.3VDC	N/A
4	TX_Dis	I	A	Transmitter Disable	LVTTL
5					
6					
7	RX+	O	C	Receiver Data	CML
8	TX+	I	B	Transmitter Data	CML
9	RX-	O	C	Receiver Data	CML
10	TX-	I	B	Transmitter Data	CML
11					
12					
13	RX+	O	R	Receiver Data	CML
14	TX+	I	A	Transmitter Data	CML
15	RX-	O	R	Receiver Data	CML
16	TX-	I	A	Transmitter Data	CML
17					
18					
19	RX+	O	W	Receiver Data	CML
20	TX+	I	N	Transmitter Data	CML
21	RX-	O	W	Receiver Data	CML
22	TX-	I	N	Transmitter Data	CML
23					
24					
25	RX+	O	L	Receiver Data	CML
26	TX+	I	M	Transmitter Data	CML
27	RX-	O	L	Receiver Data	CML
28	TX-	I	M	Transmitter Data	CML
29					
30					
31	RX_LOS	O	C	Loss Of Signal Indicator	Open Drain CMOS
32	RX_LOS	O	W	Loss Of Signal Indicator	Open Drain CMOS
33	RX_LOS	O	R	Loss Of Signal Indicator	Open Drain CMOS
34	RX_LOS	O	L	Loss Of Signal Indicator	Open Drain CMOS
35					
36					
37	TX_Dis	I	N	Transmitter Disable	LVTTL
38	GND	N/A	All	Signal Ground	Isolated from Case Ground
39	TX_Dis	I	M	Transmitter Disable	LVTTL
40	GND	N/A	All	Signal Ground	Isolated from Case Ground

*J1 center slug is isolated GND

Matrix Series MIL-DTL-38999 Optical Transceiver,
Gigabit Ethernet, Fibre Channel, ARINC 818 Applications, Multimode, 850nM

J2 ELECTRICAL PIN ASSIGNMENTS - 8TX + 8RX pattern indicated

*J2 Pin #	Symbol	I/O	J3 Pin #	Description	Logic Family
1	V_{cc}	I	All	3.3VDC	N/A
2	TX_Dis	I	D	Transmitter Disable	LVTTL
3	V_{cc}	I	All	3.3VDC	N/A
4	TX_Dis	I	S	Transmitter Disable	LVTTL
5					
6					
7	RX+	O	E	Receiver Data	CML
8	TX+	I	D	Transmitter Data	CML
9	RX-	O	E	Receiver Data	CML
10	TX-	I	D	Transmitter Data	CML
11					
12					
13	RX+	O	F	Receiver Data	CML
14	TX+	I	S	Transmitter Data	CML
15	RX-	O	F	Receiver Data	CML
16	TX-	I	S	Transmitter Data	CML
17					
18					
19	RX+	O	H	Receiver Data	CML
20	TX+	I	V	Transmitter Data	CML
21	RX-	O	H	Receiver Data	CML
22	TX-	I	V	Transmitter Data	CML
23					
24					
25	RX+	O	J	Receiver Data	CML
26	TX+	I	K	Transmitter Data	CML
27	RX-	O	J	Receiver Data	CML
28	TX-	I	K	Transmitter Data	CML
29					
30					
31	RX_LOS	O	E	Loss Of Signal Indicator	Open Drain CMOS
32	RX_LOS	O	H	Loss Of Signal Indicator	Open Drain CMOS
33	RX_LOS	O	F	Loss Of Signal Indicator	Open Drain CMOS
34	RX_LOS	O	J	Loss Of Signal Indicator	Open Drain CMOS
35					
36					
37	TX_Dis	I	V	Transmitter Disable	LVTTL
38	GND	N/A	All	Signal Ground	Isolated from Case Ground
39	TX_Dis	I	K	Transmitter Disable	LVTTL
40	GND	N/A	All	Signal Ground	Isolated from Case Ground

*J2 center slug is isolated GND

Matrix Series MIL-DTL-38999 Optical Transceiver,
Gigabit Ethernet, Fibre Channel, ARINC 818 Applications, Multimode, 850nM

J1 ELECTRICAL PIN ASSIGNMENTS - 16TX pattern indicated

*J1 Pin #	Symbol	I/O	J3 Pin #	Description	Logic Family
1	V_{CC}	I	All	3.3VDC	N/A
2	TX_Dis	I	B	Transmitter Disable	LVTTL
3	V_{CC}	I	All	3.3VDC	N/A
4	TX_Dis	I	A	Transmitter Disable	LVTTL
5					
6					
7	TX+	I	C	Transmitter Data	CML
8	TX+	I	B	Transmitter Data	CML
9	TX-	I	C	Transmitter Data	CML
10	TX-	I	B	Transmitter Data	CML
11					
12					
13	TX+	I	R	Transmitter Data	CML
14	TX+	I	A	Transmitter Data	CML
15	TX-	I	R	Transmitter Data	CML
16	TX-	I	A	Transmitter Data	CML
17					
18					
19	TX+	I	W	Transmitter Data	CML
20	TX+	I	N	Transmitter Data	CML
21	TX-	I	W	Transmitter Data	CML
22	TX-	I	N	Transmitter Data	CML
23					
24					
25	TX+	I	L	Transmitter Data	CML
26	TX+	I	M	Transmitter Data	CML
27	TX-	I	L	Transmitter Data	CML
28	TX-	I	M	Transmitter Data	CML
29					
30					
31	TX_Dis	I	C	Transmitter Disable	LVTTL
32	TX_Dis	I	W	Transmitter Disable	LVTTL
33	TX_Dis	I	R	Transmitter Disable	LVTTL
34	TX_Dis	I	L	Transmitter Disable	LVTTL
35					
36					
37	TX_Dis	I	N	Transmitter Disable	LVTTL
38	GND	N/A	All	Signal Ground	Isolated from Case Ground
39	TX_Dis	I	M	Transmitter Disable	LVTTL
40	GND	N/A	All	Signal Ground	Isolated from Case Ground

*J1 center slug is isolated GND

Matrix Series MIL-DTL-38999 Optical Transceiver,
Gigabit Ethernet, Fibre Channel, ARINC 818 Applications, Multimode, 850nM

J2 ELECTRICAL PIN ASSIGNMENTS - 16TX pattern indicated

*J2 Pin #	Symbol	I/O	J3 Pin #	Description	Logic Family
1	V_{CC}	I	All	3.3VDC	N/A
2	TX_Dis	I	D	Transmitter Disable	LVTTL
3	V_{CC}	I	All	3.3VDC	N/A
4	TX_Dis	I	S	Transmitter Disable	LVTTL
5					
6					
7	TX+	I	E	Transmitter Data	CML
8	TX+	I	D	Transmitter Data	CML
9	TX-	I	E	Transmitter Data	CML
10	TX-	I	D	Transmitter Data	CML
11					
12					
13	TX+	I	F	Transmitter Data	CML
14	TX+	I	S	Transmitter Data	CML
15	TX-	I	F	Transmitter Data	CML
16	TX-	I	S	Transmitter Data	CML
17					
18					
19	TX+	I	H	Transmitter Data	CML
20	TX+	I	V	Transmitter Data	CML
21	TX-	I	H	Transmitter Data	CML
22	TX-	I	V	Transmitter Data	CML
23					
24					
25	TX+	I	J	Transmitter Data	CML
26	TX+	I	K	Transmitter Data	CML
27	TX-	I	J	Transmitter Data	CML
28	TX-	I	K	Transmitter Data	CML
29					
30					
31	TX_Dis	I	E	Transmitter Disable	LVTTL
32	TX_Dis	I	H	Transmitter Disable	LVTTL
33	TX_Dis	I	F	Transmitter Disable	LVTTL
34	TX_Dis	I	J	Transmitter Disable	LVTTL
35					
36					
37	TX_Dis	I	V	Transmitter Disable	LVTTL
38	GND	N/A	All	Signal Ground	Isolated from Case Ground
39	TX_Dis	I	K	Transmitter Disable	LVTTL
40	GND	N/A	All	Signal Ground	Isolated from Case Ground

*J2 center slug is isolated GND

Matrix Series MIL-DTL-38999 Optical Transceiver,
Gigabit Ethernet, Fibre Channel, ARINC 818 Applications, Multimode, 850nM

J1 ELECTRICAL PIN ASSIGNMENTS - 16RX pattern indicated

*J1 Pin #	Symbol	I/O	J3 Pin #	Description	Logic Family
1	V_{CC}	I	All	3.3VDC	N/A
2	RX_LOS	O	B	Loss Of Signal Indicator	Open Drain CMOS
3	V_{CC}	I	All	3.3VDC	N/A
4	RX_LOS	O	A	Loss Of Signal Indicator	Open Drain CMOS
5					
6					
7	RX+	O	C	Receiver Data	CML
8	RX+	O	B	Receiver Data	CML
9	RX-	O	C	Receiver Data	CML
10	RX-	O	B	Receiver Data	CML
11					
12					
13	RX+	O	R	Receiver Data	CML
14	RX+	O	A	Receiver Data	CML
15	RX-	O	R	Receiver Data	CML
16	RX-	O	A	Receiver Data	CML
17					
18					
19	RX+	O	W	Receiver Data	CML
20	RX+	O	N	Receiver Data	CML
21	RX-	O	W	Receiver Data	CML
22	RX-	O	N	Receiver Data	CML
23					
24					
25	RX+	O	L	Receiver Data	CML
26	RX+	O	M	Receiver Data	CML
27	RX-	O	L	Receiver Data	CML
28	RX-	O	M	Receiver Data	CML
29					
30					
31	RX_LOS	O	C	Loss Of Signal Indicator	Open Drain CMOS
32	RX_LOS	O	W	Loss Of Signal Indicator	Open Drain CMOS
33	RX_LOS	O	R	Loss Of Signal Indicator	Open Drain CMOS
34	RX_LOS	O	L	Loss Of Signal Indicator	Open Drain CMOS
35					
36					
37	RX_LOS	O	N	Loss Of Signal Indicator	Open Drain CMOS
38	GND	N/A	All	Signal Ground	Isolated from Case Ground
39	RX_LOS	O	M	Loss Of Signal Indicator	Open Drain CMOS
40	GND	N/A	All	Signal Ground	Isolated from Case Ground

*J1 center slug is isolated GND

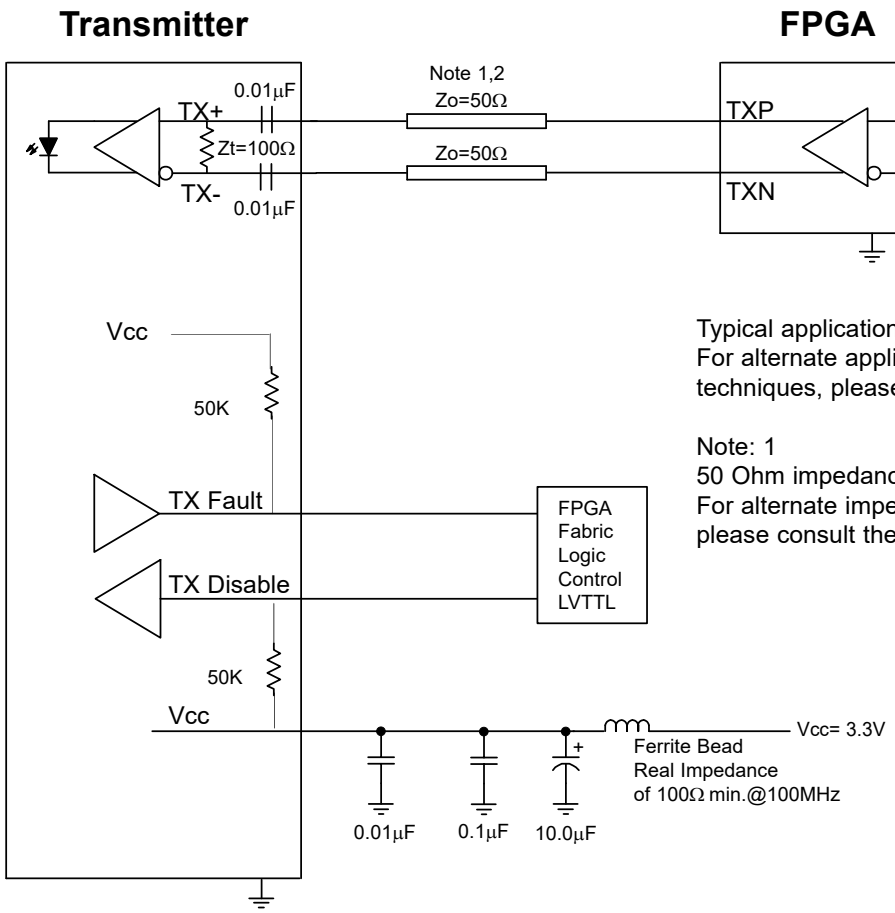
J2 ELECTRICAL PIN ASSIGNMENTS - 16RX pattern indicated

*J2 Pin #	Symbol	I/O	J3 Pin #	Description	Logic Family
1	V_{CC}	I	All	3.3VDC	N/A
2	RX_LOS	O	D	Loss Of Signal Indicator	Open Drain CMOS
3	V_{CC}	I	All	3.3VDC	N/A
4	RX_LOS	O	S	Loss Of Signal Indicator	Open Drain CMOS
5					
6					
7	RX+	O	E	Receiver Data	CML
8	RX+	O	D	Receiver Data	CML
9	RX-	O	E	Receiver Data	CML
10	RX-	O	D	Receiver Data	CML
11					
12					
13	RX+	O	F	Receiver Data	CML
14	RX+	O	S	Receiver Data	CML
15	RX-	O	F	Receiver Data	CML
16	RX-	O	S	Receiver Data	CML
17					
18					
19	RX+	O	H	Receiver Data	CML
20	RX+	O	V	Receiver Data	CML
21	RX-	O	H	Receiver Data	CML
22	RX-	O	V	Receiver Data	CML
23					
24					
25	RX+	O	J	Receiver Data	CML
26	RX+	O	K	Receiver Data	CML
27	RX-	O	J	Receiver Data	CML
28	RX-	O	K	Receiver Data	CML
29					
30					
31	RX_LOS	O	E	Loss Of Signal Indicator	Open Drain CMOS
32	RX_LOS	O	H	Loss Of Signal Indicator	Open Drain CMOS
33	RX_LOS	O	F	Loss Of Signal Indicator	Open Drain CMOS
34	RX_LOS	O	J	Loss Of Signal Indicator	Open Drain CMOS
35					
36					
37	RX_LOS	O	V	Loss Of Signal Indicator	Open Drain CMOS
38	GND	N/A	All	Signal Ground	Isolated from Case Ground
39	RX_LOS	O	K	Loss Of Signal Indicator	Open Drain CMOS
40	GND	N/A	All	Signal Ground	Isolated from Case Ground

*J2 center slug is isolated GND

TRANSMITTER APPLICATION SCHEMATIC

For Xilinx Rocket I/O Interfaces



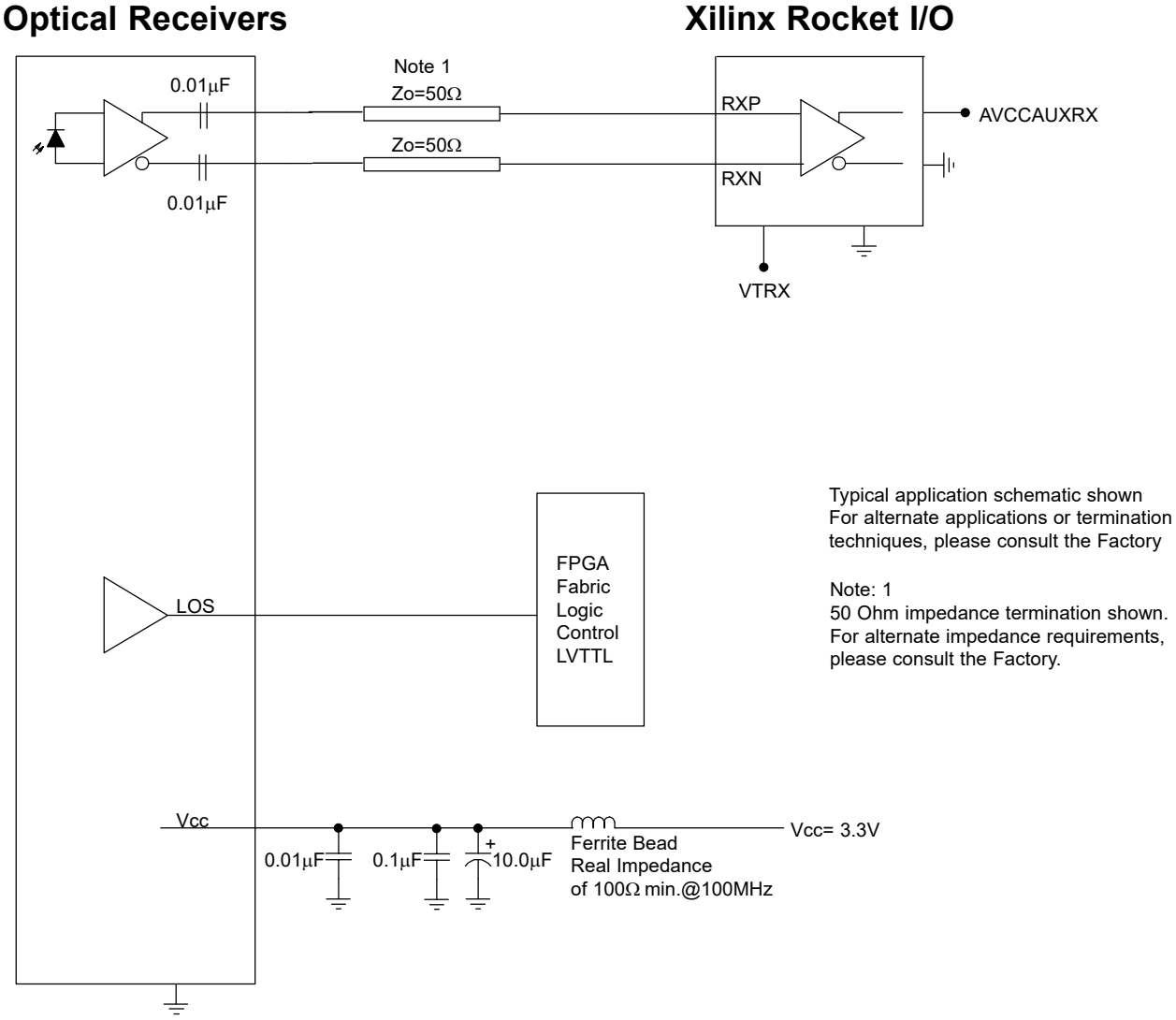
Typical application schematic shown
For alternate applications or termination techniques, please consult the Factory

Note: 1
50 Ohm impedance termination shown.
For alternate impedance requirements, please consult the Factory.

Matrix Series MIL-DTL-38999 Optical Transceiver,
Gigabit Ethernet, Fibre Channel, ARINC 818 Applications, Multimode, 850nM

RECEIVER APPLICATION SCHEMATIC

For Xilinx Rocket I/O Interfaces



Typical application schematic shown
For alternate applications or termination techniques, please consult the Factory

Note: 1
50 Ohm impedance termination shown.
For alternate impedance requirements, please consult the Factory.

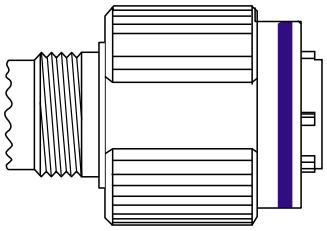
APPENDIX A1

MIL-DTL-38999 FIBER OPTIC CABLE PLUG / MIL-T-29504 RECEPTACLE TERMINI

*See DSCC or SAE QPL for Approved Suppliers
http://www.dscc.dla.mil/programs/qmlqpl/QPLdetail.asp?QPL=38999

*D38999 PLUG - RECEPTACLE INSERT

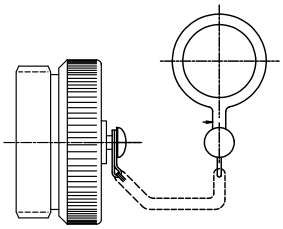
MIL-DTL-38999 CABLE PLUG	
MS PLUG P/N	*D38999/26xH21SN



x = Service Class

*CABLE PROTECTION CAP

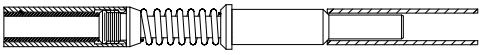
D38999/32 PLUG PROTECTION CAP	
MS PLUG CAP P/N	*D38999/32x17N



x = Service Class

*FIBER OPTIC TERMINUS

M29504 RECEPTACLE TERMINUS	
RECEPTACLE	*M29504/05-xxxx**

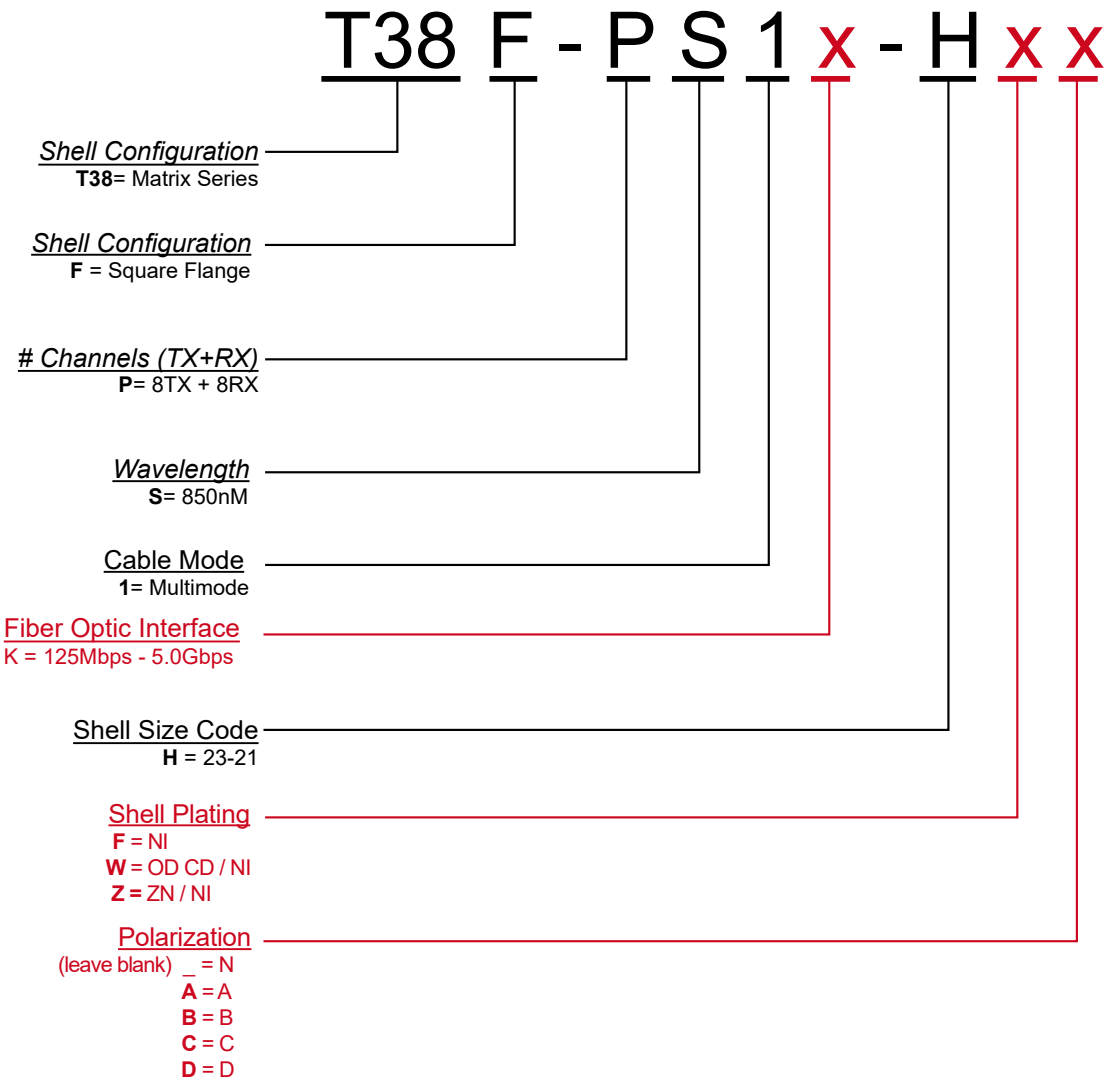


**defined by fiber optic cable configuration

APPENDIX A2

PART NUMBER OPTIONS

Matrix Optical Transceivers



MOOG PROTOKRAFT

192 Bob Fitz Road, Johnson City, TN 37615
salesmp@moog.com
moogprotokraft.com